2812 #4

Docket No. 217760US2S

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Motoshige KOBAYASHI et al.

SERIAL NO: 10/025,744 GAU: 2812

FILED: 12/26/01 EXAMINER:

FOR: SEMICONDUCTOR DEVICE

INFORMATION DISCLOSURE/RELATED CASE STATEMENT UNDER 37 CFR 1.97

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR!

Applicant(s) wish to disclose the following information.

REFERENCES

- ☐ The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.
- ☐ A check is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

- ■ Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the claims and drawings of the pending application(s) is attached.
- ☐ A check is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

- ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.
- ■ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

- ■ Please charge any additional fees for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

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I:\em\EMRel\217s218s\217760US Transmittal Letter (Abby).wpd

LIST OF RELATED CASES

Docket Number	Serial or Patent No.	Filing or Issue Date	Status or Patentee
217760US2S*	10/025,744	12/26/01	PENDING
221406US2S	10/107,405	03/28/02	PENDING

*Present application; listed for information

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WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a first base layer having a first conductivity type, said first base layer having first and second surfaces and further having a high resistance;

a second base layer, provided in said first surface, having a second conductivity type;

an emitter layer, provided in said second base layer, having said first conductivity type;

a gate electrode provided through a gate insulating film over said second base layer disposed between said emitter layer and said first base layer;

a buffer layer, formed in said second surface, having said first conductivity type and further having a high impurity concentration;

a first activation rate, defined by an activated first conductivity type impurity density [cm^{-2}] in said buffer layer due to SR analysis/a first conductivity type impurity density [cm^{-2}] in said buffer layer due to SIMS analysis, being 25% or more;

a collector layer, provided in said buffer layer, having said second conductivity type; and

a second activation rate, defined by an activated second conductivity type impurity density [cm^{-2}] in said collector layer due to SR analysis/a second conductivity type impurity density [cm^{-2}] in said collector layer due to SIMS analysis, being more than

0% and 10% or less.

2. The semiconductor device according to claim 1, wherein the dose of the second conductivity type impurity in said buffer layer positioned within 2 μm from the surface of said collector layer is 1×10^{15} cm^{-2} or more.

3. The semiconductor device according to claim 1, wherein said buffer layer is provided in said first base layer formed within 2 μm from the surface of said collector layer.

4. The semiconductor device according to claim 3, wherein the dose of the second conductivity type impurity in said buffer layer positioned within 2 μm from the surface of said collector layer is 1×10^{15} cm^{-2} or more.

5. A method of manufacturing a semiconductor device, comprising:

preparing a first base layer having a first conductivity type and also having first and second surfaces, said first base layer having a high resistance;

successively depositing an insulating film providing a gate insulating film and a conductive film providing a gate electrode on said first surface of the first base layer;

successively patterning said conductive film and said insulating film to expose partly said first

surface;

forming a second base layer having a second conductivity type in the exposed first surface by self-alignment;

selectively forming an emitter layer having said first conductivity type in said second base layer;

forming an emitter electrode on said emitter layer;

implanting first impurity ions having said first conductivity type into said second surface;

activating said first impurity ions by first annealing to form a buffer layer having a high impurity concentration and also having said first conductivity type on said second surface;

implanting second impurity ions having said second conductivity type into a said buffer layer; and

activating said second impurity ions by second annealing to form a collector layer having said second conductivity type in said buffer layer.

6. The method according to claim 5, wherein:

a first activation rate, defined by an activated first conductivity type impurity density [cm^{-2}] in said buffer layer due to SR analysis/a first conductivity type impurity density [cm^{-2}] in said buffer layer due to SIMS analysis, is 25% or more; and

a second activation rate, defined by an activated second conductivity type impurity density [cm^{-2}] in

said collector layer due to SR analysis/a second conductivity type impurity density [cm^{-2}] in said collector layer due to SIMS analysis, is more than 0% and 10% or less.

7. The method according to claim 5, wherein said second annealing is carried out at a temperature lower than the temperature for said first annealing.

8. The method according to claim 5, wherein the temperature for said second annealing is lower than the temperature for maintaining a quality of a passivation film.

9. The method according to claim 5, wherein said first annealing is laser annealing, and said second annealing is furnace annealing.

10. The method according to claim 5, wherein said second impurity ions are implanted into said buffer layer with the dose for making said collector layer amorphous.

ABSTRACT OF THE DISCLOSURE

A semiconductor device comprises a first base layer for providing a PT-IGBT or IEGT structure, which includes a buffer layer and a collector layer provided in the buffer layer. A first activation rate, defined by an activated first conductivity type impurity density [cm^{-2}] in the buffer layer due to SR analysis/ a first conductivity type impurity density [cm^{-2}] in the buffer layer due to SIMS analysis is given by 25% or more, and a second activation rate, defined by an activated second conductivity type impurity density [cm^{-2}] in the collector layer due to SR analysis/a second conductivity type impurity density [cm^{-2}] in the collector layer duet to SIMS analysis is given by more than 0% and 10% or less.

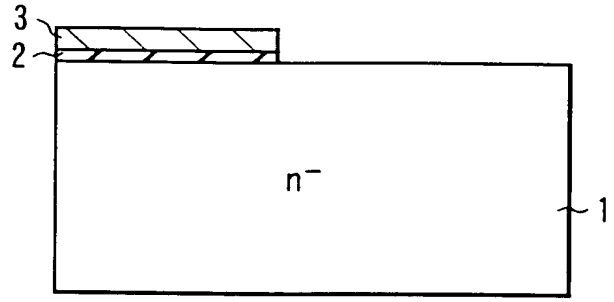

FIG. 1A

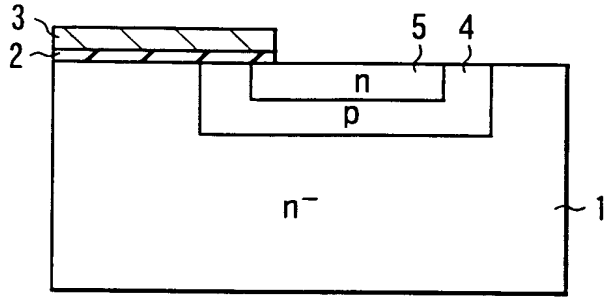

FIG. 1B

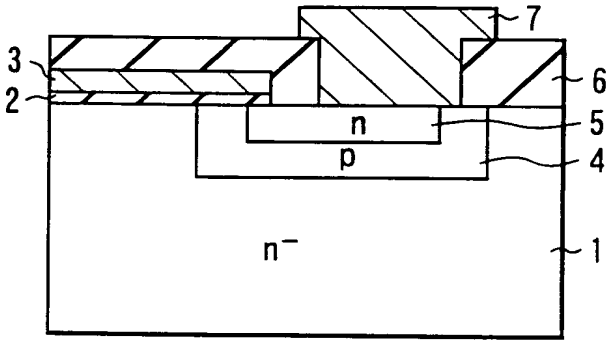

FIG. 1C

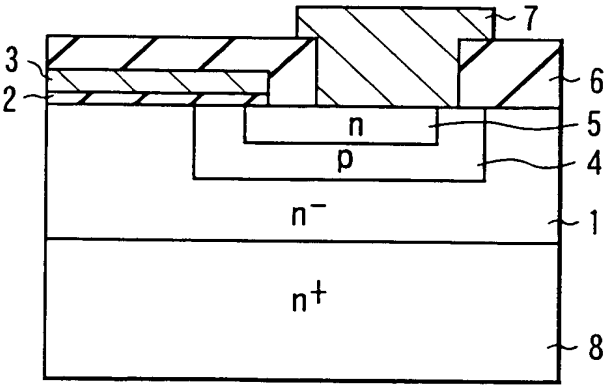

FIG. 1D

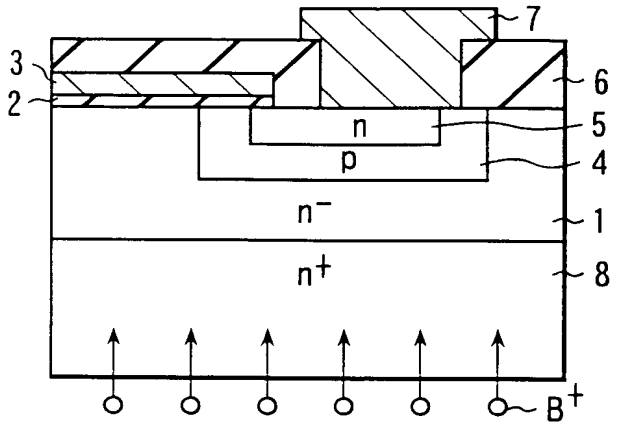

FIG. 1E

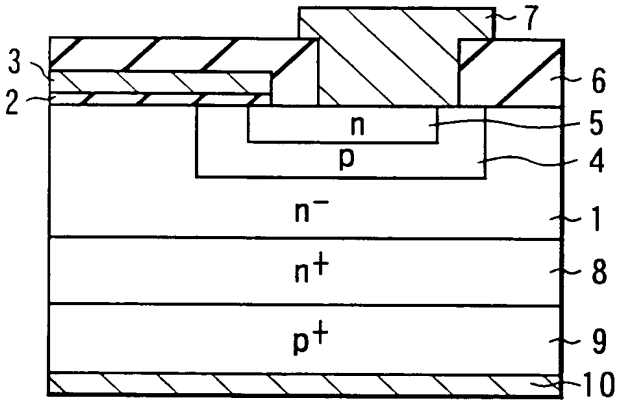

FIG. 1F

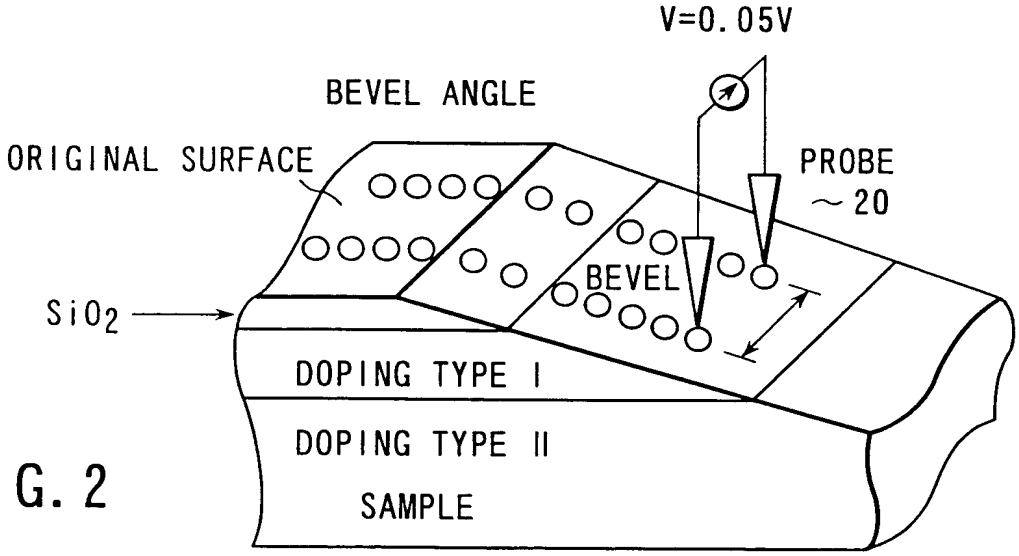

FIG. 2

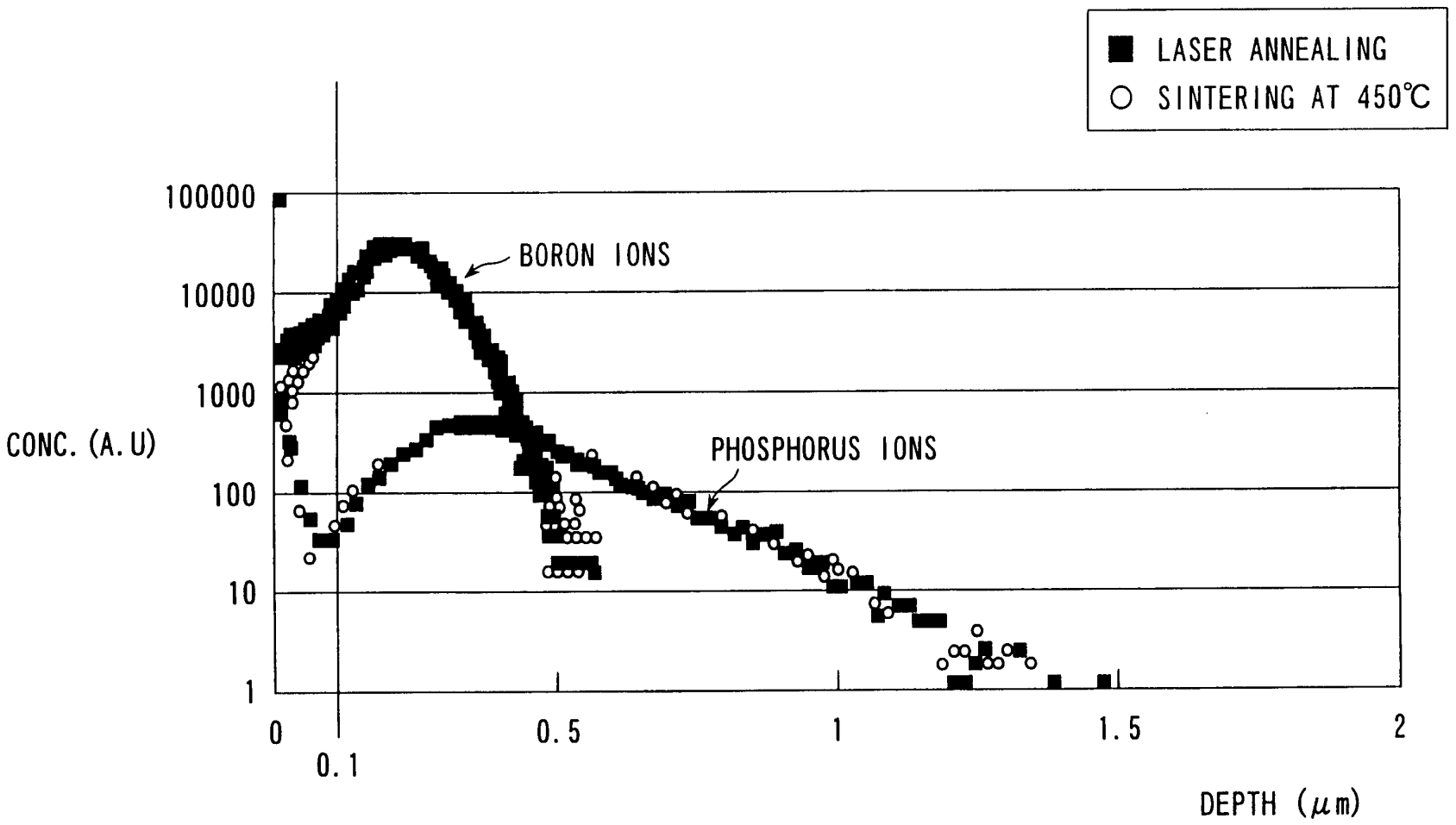
LASER ANNEALING
SINTERING AT 450℃
100000
10000
1000
100
10
1
CONC. (A.U)
BORON IONS
PHOSPHORUS IONS
0
0.1
0.5
1
1.5
2
DEPTH (μm)

FIG. 3

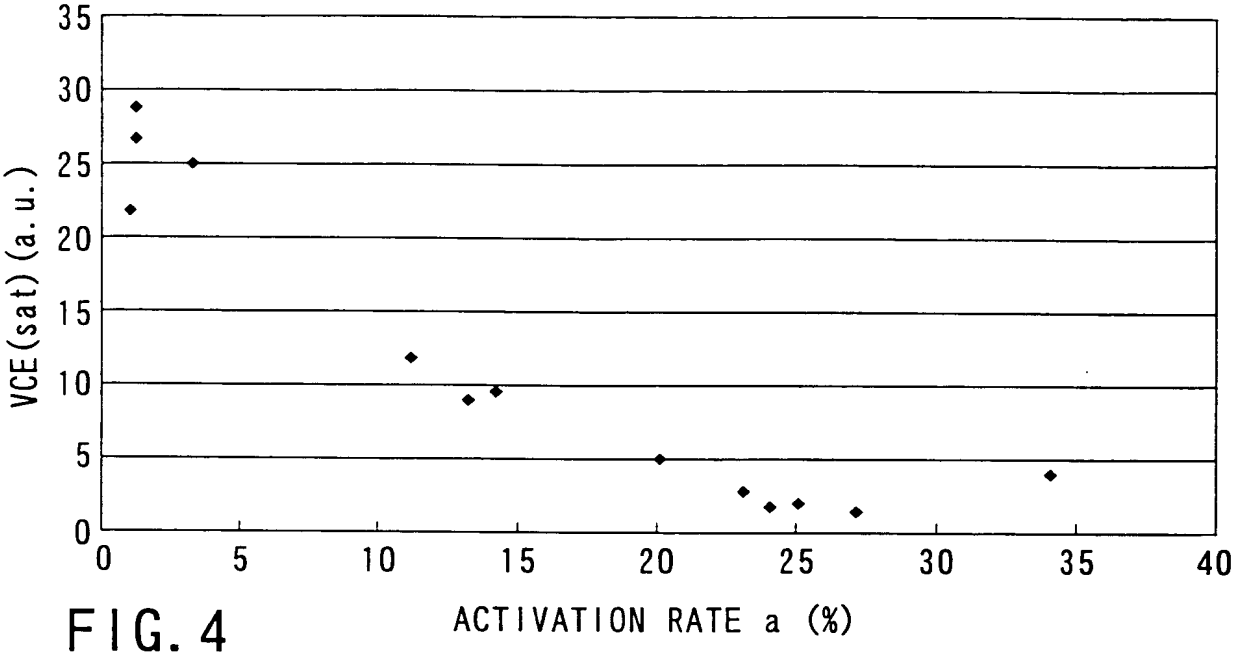

FIG. 4

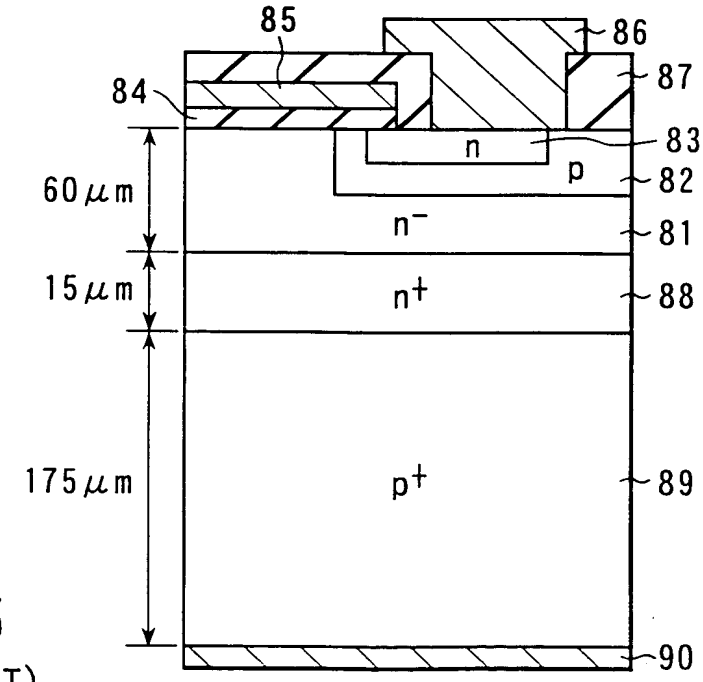

FIG. 5
(PRIOR ART)

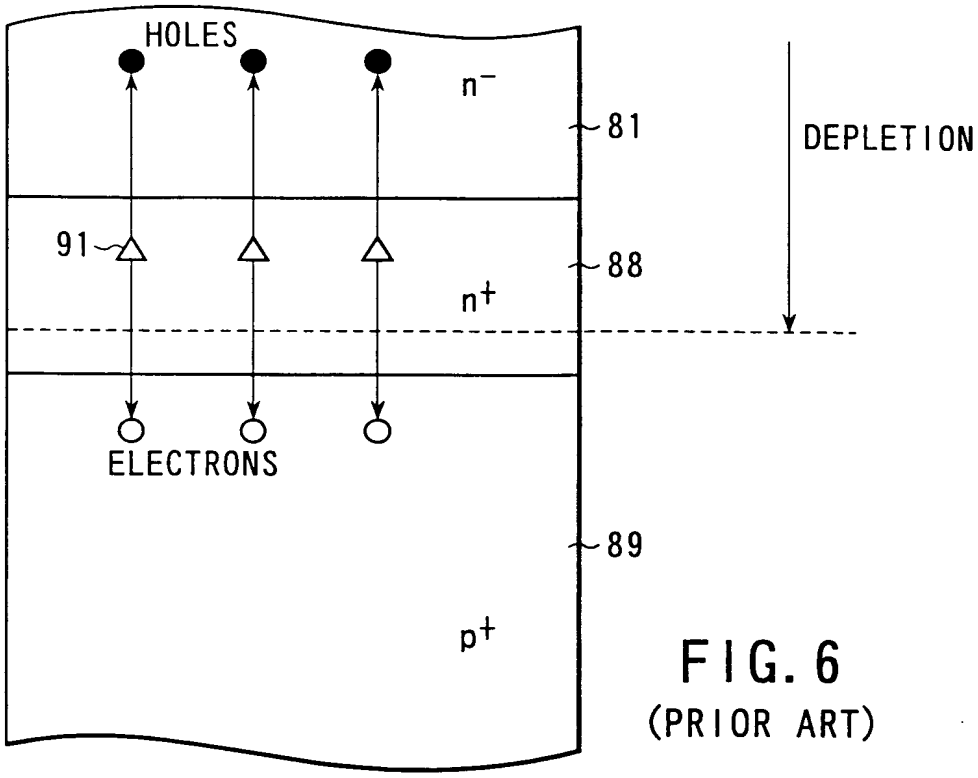

FIG. 6
(PRIOR ART)

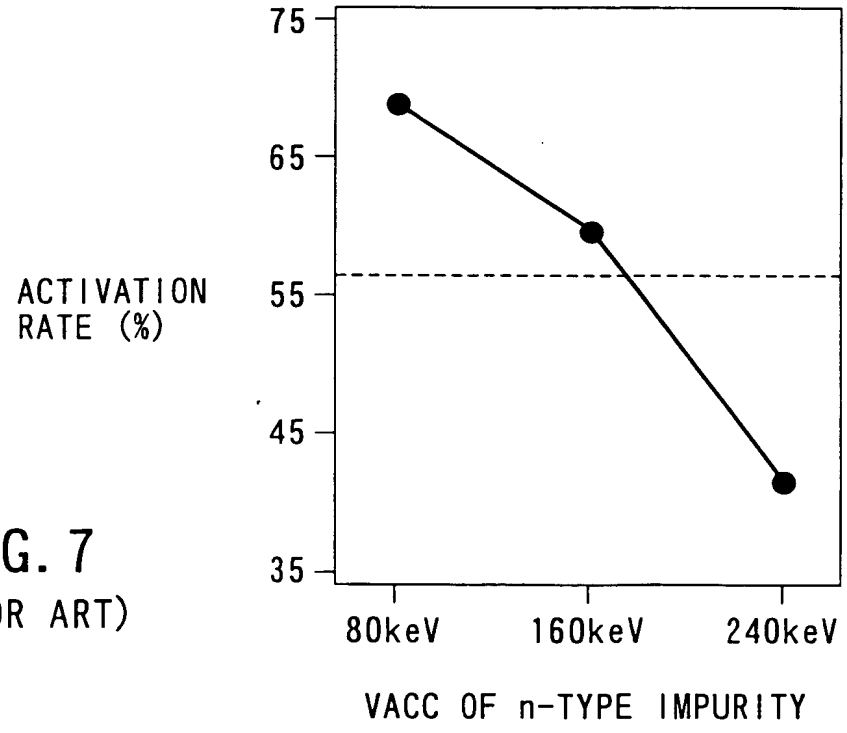

FIG. 7
(PRIOR ART)